

## 65V N-Ch Power MOSFET

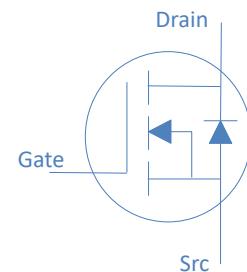
### Feature

- ◊ High Speed Power Switching, Logic level
- ◊ Enhanced Body diode dv/dt capability
- ◊ Enhanced Avalanche Ruggedness
- ◊ 100% UIS Tested, 100% Rg Tested
- ◊ Lead Free, Halogen Free

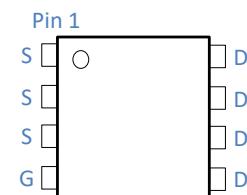
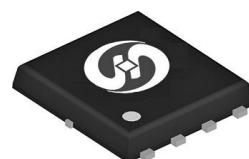
$V_{DS}$	65	V
$R_{DS(on),typ}$	$V_{GS}=10V$	7.5 mΩ
$R_{DS(on),typ}$	$V_{GS}=4.5V$	10.5 mΩ
$I_D$ (Silicon Limited)	55	A
$I_D$ (Package Limited)	30	A

### Application

- ◊ Synchronous Rectification in SMPS
- ◊ Hard Switching and High Speed Circuit
- ◊ DC/DC in Telecoms and Industrial



DFN5\*6



Part Number	Package	Marking
HGN090NE6AL	DFN5*6	GN090NE6AL

### Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25^\circ\text{C}$	55	A
Continuous Drain Current (Package Limited)		$T_C=100^\circ\text{C}$	35	
Continuous Drain Current		$T_C=25^\circ\text{C}$	30	
Drain to Source Voltage	$V_{DS}$	-	65	V
Gate to Source Voltage	$V_{GS}$	-	$\pm 20$	V
Pulsed Drain Current	$I_{DM}$	-	270	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.4\text{mH}, T_C=25^\circ\text{C}$	45	mJ
Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	50	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 150	°C

### Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	55	°C/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	2.5	°C/W

**Electrical Characteristics at  $T_j=25^\circ\text{C}$  (unless otherwise specified)**
**Static Characteristics**

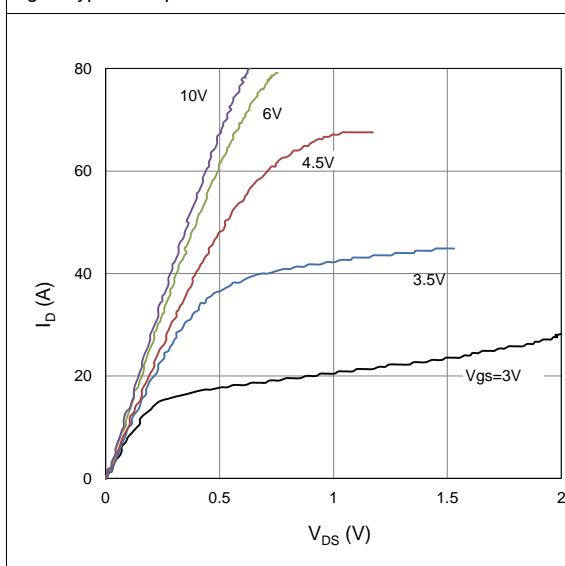
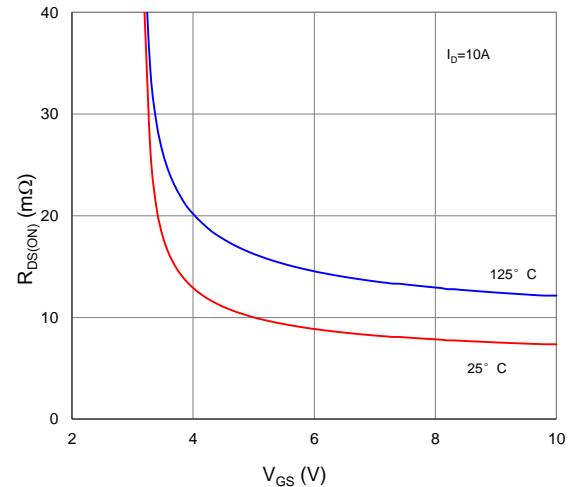
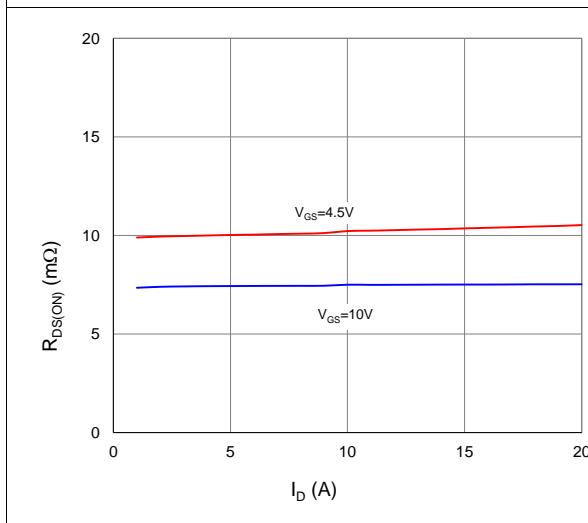
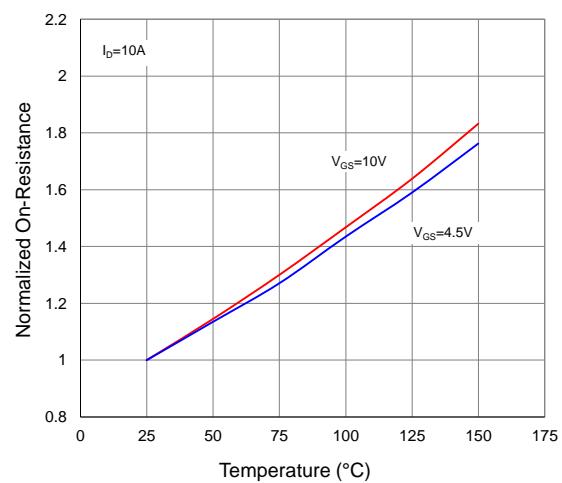
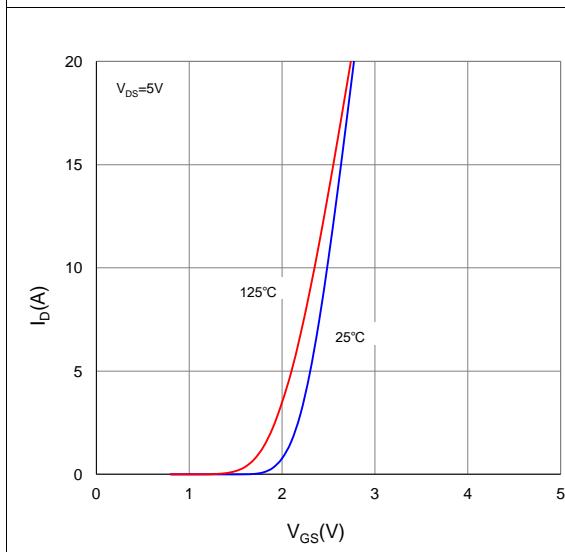
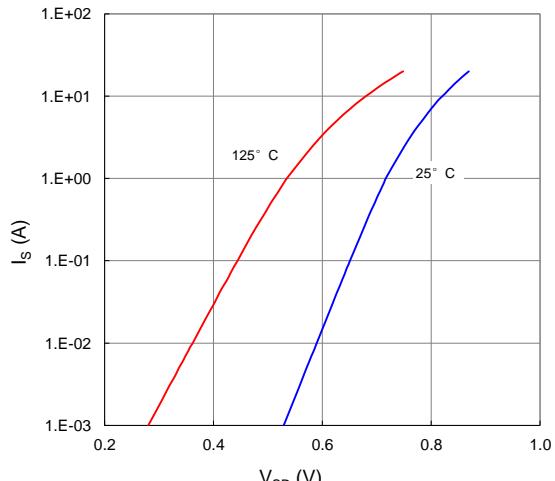
Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_D=250\mu\text{A}$	65	-	-	V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}, I_D=250\mu\text{A}$	1.0	1.6	2.4	
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=60\text{V}, T_j=25^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=60\text{V}, T_j=100^\circ\text{C}$	-	-	100	
Gate to Source Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}}=\pm20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	$\pm100$	nA
Drain to Source on Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=10\text{V}, I_D=10\text{A}$	-	7.5	9	$\text{m}\Omega$
Drain to Source on Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=4.5\text{V}, I_D=5\text{A}$	-	10.5	13	$\text{m}\Omega$
Transconductance	$g_{\text{fs}}$	$V_{\text{DS}}=5\text{V}, I_D=10\text{A}$	-	29	-	S
Gate Resistance	$R_G$	$V_{\text{GS}}=0\text{V}, V_{\text{DS}} \text{ Open}, f=1\text{MHz}$	-	1.4	-	$\Omega$

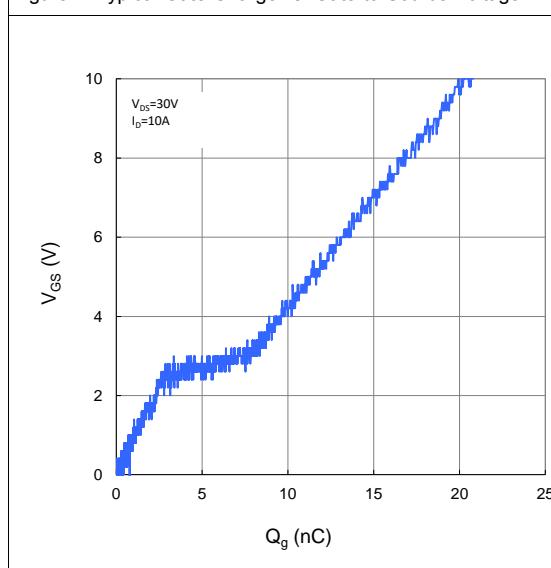
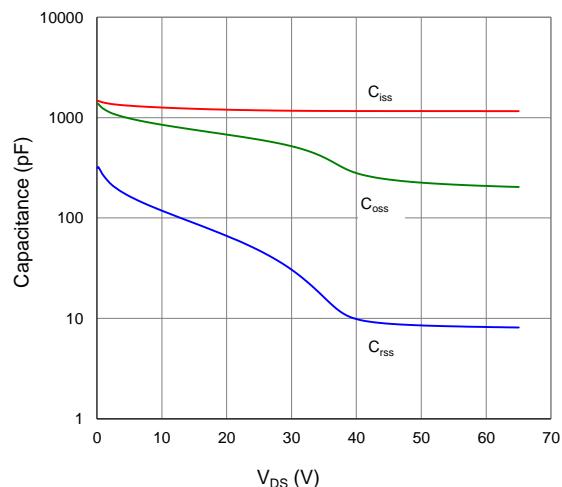
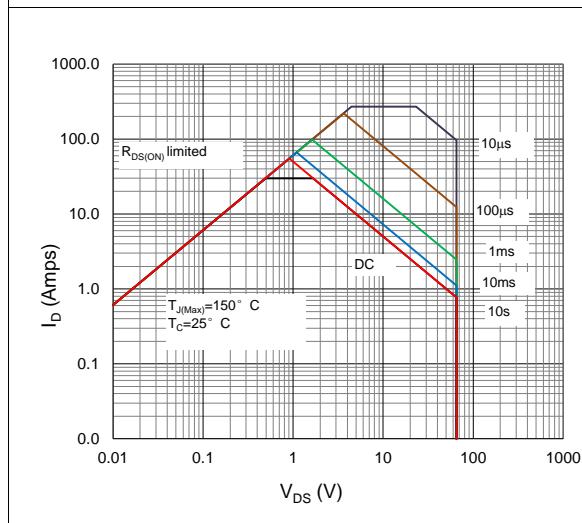
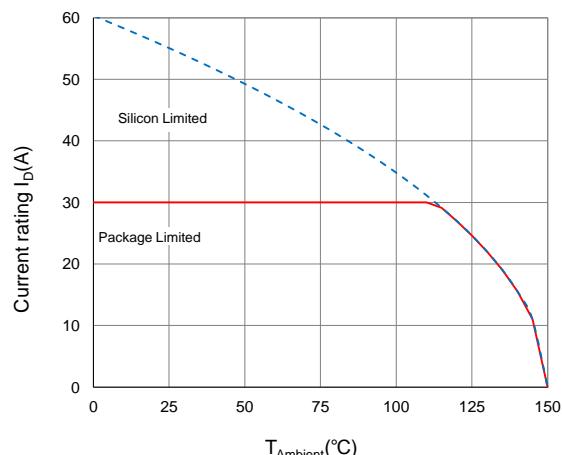
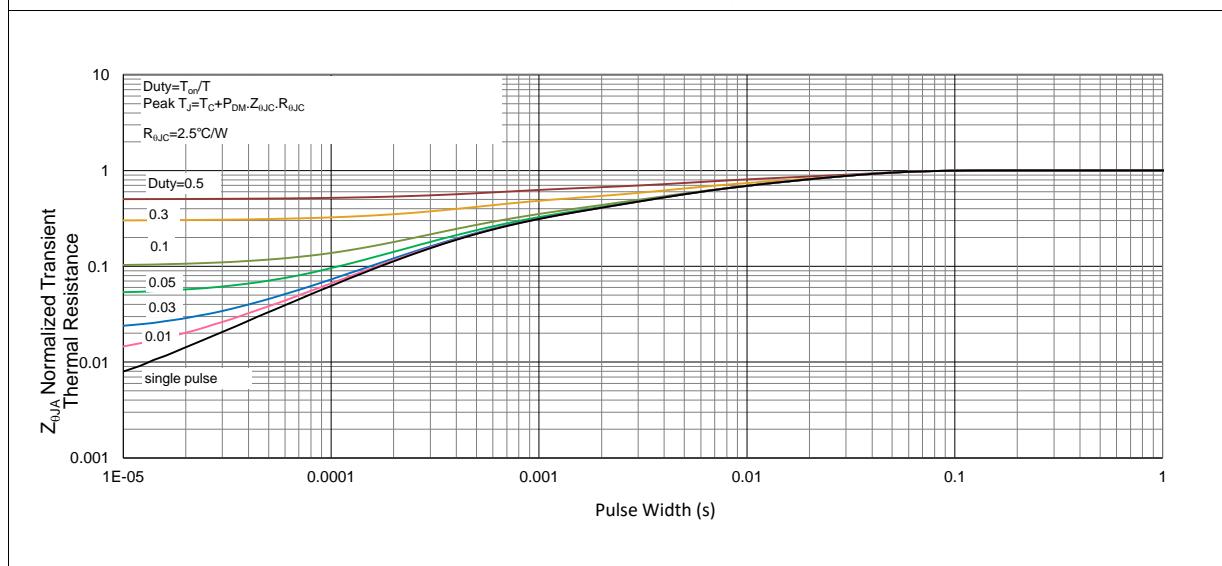
**Dynamic Characteristics**

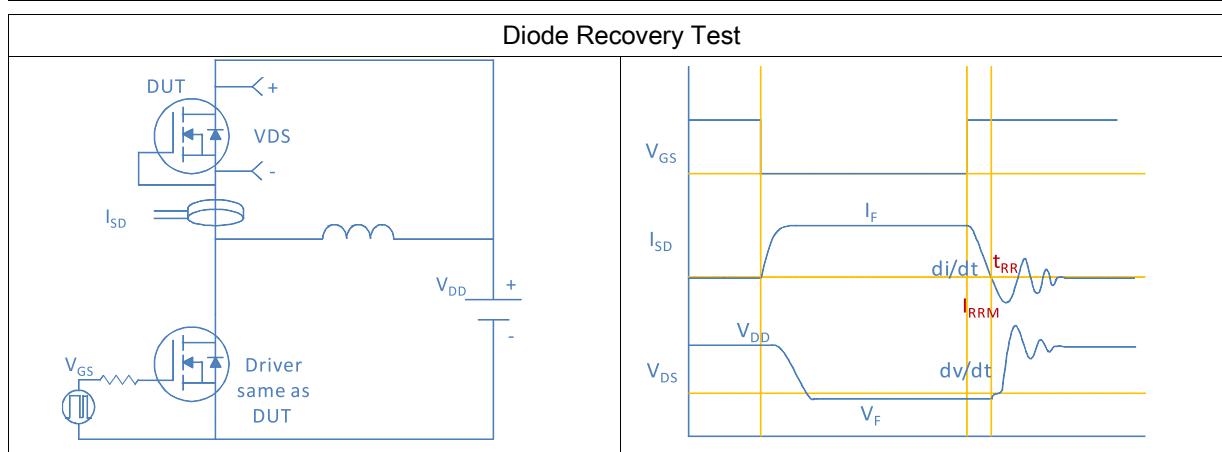
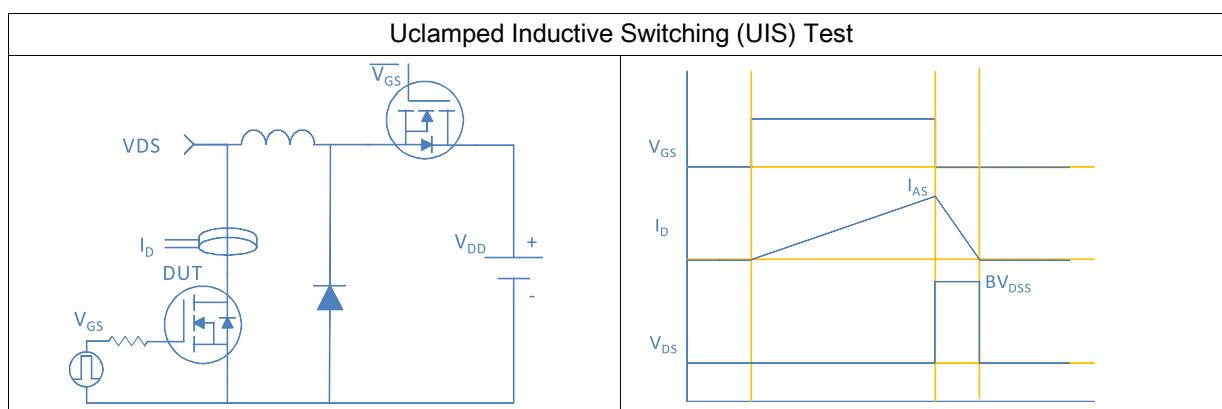
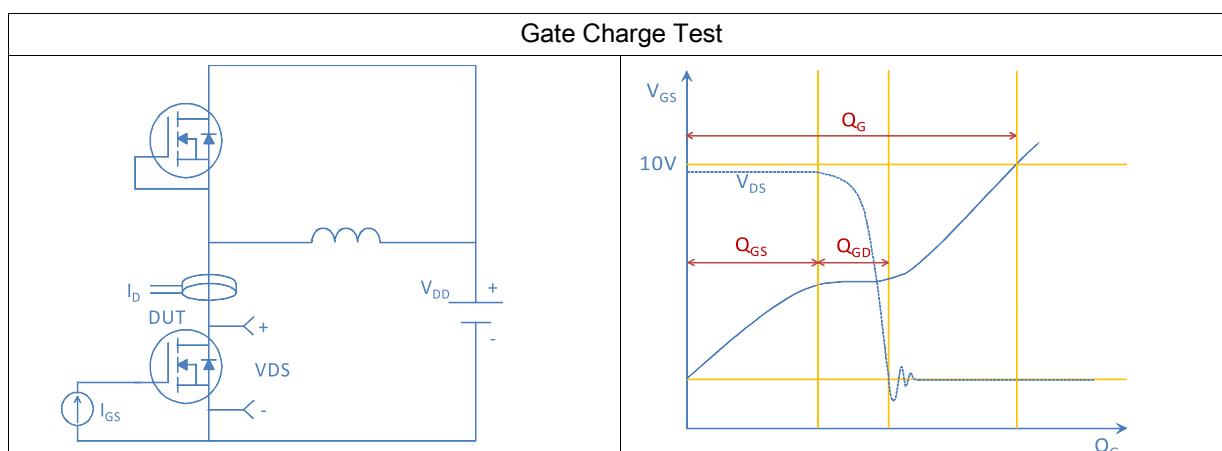
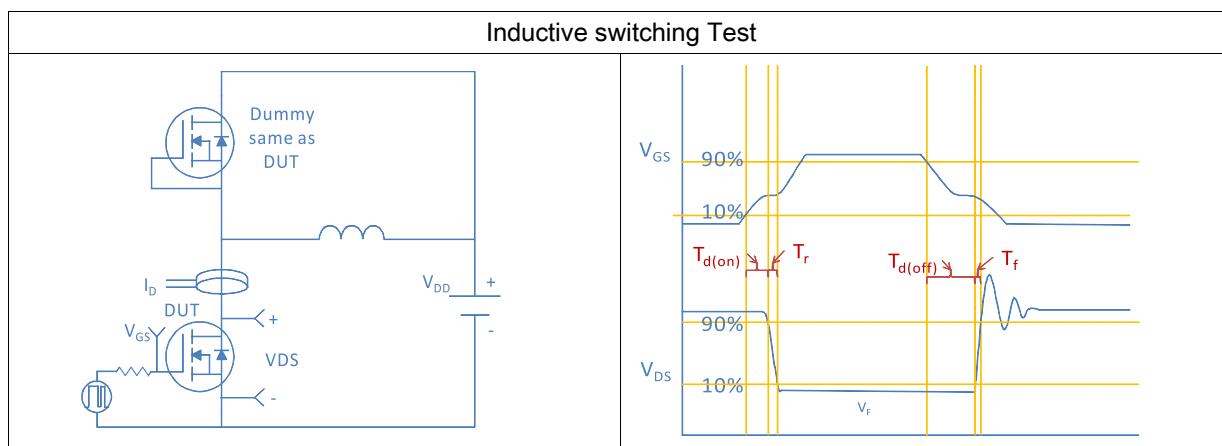
Input Capacitance	$C_{\text{iss}}$	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=30\text{V}, f=1\text{MHz}$	-	1170	-	pF
Output Capacitance	$C_{\text{oss}}$		-	518	-	
Reverse Transfer Capacitance	$C_{\text{rss}}$		-	31	-	
Total Gate Charge	$Q_g(10\text{V})$	$V_{\text{DD}}=30\text{V}, I_D=10\text{A}, V_{\text{GS}}=10\text{V}$	-	20.5	-	nC
Total Gate Charge	$Q_g(4.5\text{V})$		-	10.5	-	
Gate to Source Charge	$Q_{\text{gs}}$		-	2.5	-	
Gate to Drain (Miller) Charge	$Q_{\text{gd}}$		-	5.5	-	
Turn on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=30\text{V}, I_D=10\text{A}, V_{\text{GS}}=10\text{V}, R_G=10\Omega$	-	7	-	ns
Rise time	$t_r$		-	4	-	
Turn off Delay Time	$t_{\text{d}(\text{off})}$		-	22	-	
Fall Time	$t_f$		-	5	-	

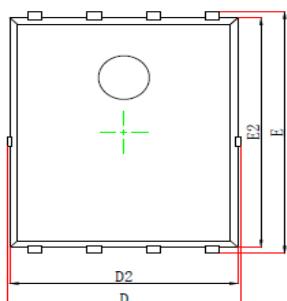
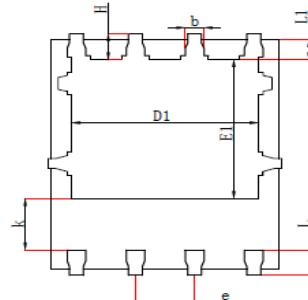
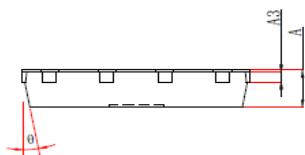
**Reverse Diode Characteristics**

Diode Forward Voltage	$V_{\text{SD}}$	$V_{\text{GS}}=0\text{V}, I_F=20\text{A}$	-	0.9	1.2	V
Reverse Recovery Time	$t_{\text{rr}}$	$V_R=30\text{V}, I_F=10\text{A}, dI_F/dt=100\text{A}/\mu\text{s}$	-	33	-	ns
Reverse Recovery Charge	$Q_{\text{rr}}$		-	24	-	nC

**Fig 1. Typical Output Characteristics**

**Figure 2. On-Resistance vs. Gate-Source Voltage**

**Figure 3. On-Resistance vs. Drain Current and Gate Voltage**

**Figure 4. Normalized On-Resistance vs. Junction Temperature**

**Figure 5. Typical Transfer Characteristics**

**Figure 6. Typical Source-Drain Diode Forward Voltage**


**Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage**

**Figure 8. Typical Capacitance vs. Drain-to-Source Voltage**

**Figure 9. Maximum Safe Operating Area**

**Figure 10. Maximum Drain Current vs. Case Temperature**

**Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient**




**Package Outline**
**DFN5x6\_P, 8 Leads**

Top View  
[顶视图]

Bottom View  
[背视图]

Side View  
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A3	0.254	REF	0.010	REF
D	4.680	5.120	0.184	0.202
E	5.900	6.126	0.232	0.241
D1	3.610	4.110	0.142	0.162
E1	3.380	3.780	0.133	0.149
D2	4.800	5.000	0.189	0.197
E2	5.674	5.826	0.223	0.229
k	1.100	1.390	0.043	0.055
b	0.330	0.510	0.013	0.020
e	1.270TYP		1.270TYP	
L	0.510	0.711	0.020	0.028
L1	0.424	0.576	0.017	0.023
H	0.410	0.726	0.016	0.029
$\theta$	$0^\circ$	$12^\circ$	$0^\circ$	$12^\circ$